



From CMOS to CMORE: innovation on a MEMS platform

Presenter: Jo De Boeck, Senior VP and CTO imec international

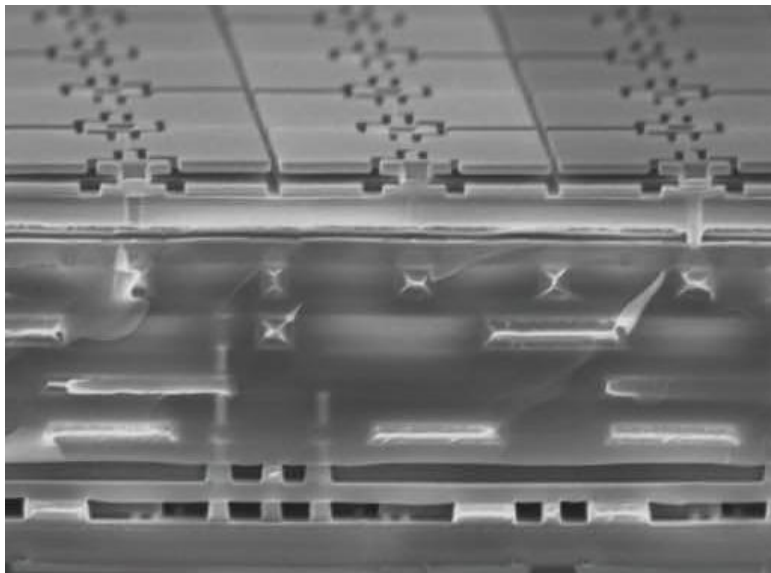
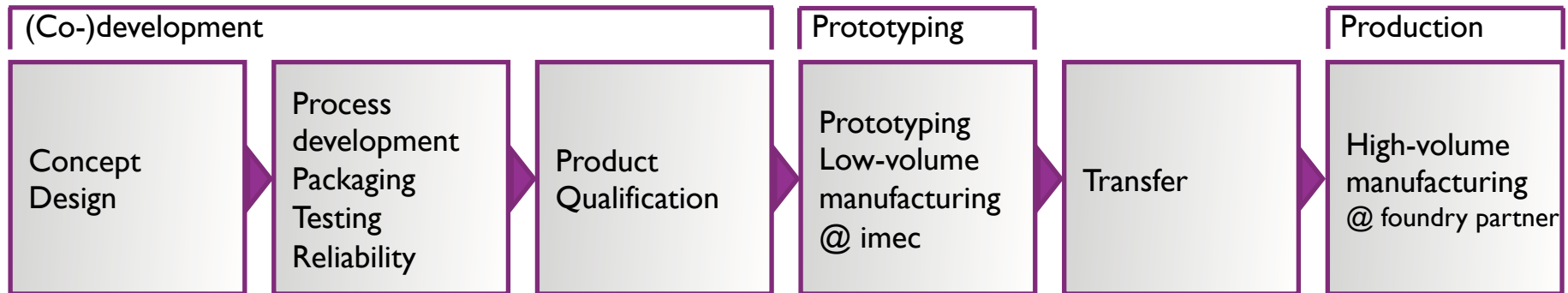
Rudi Cartuyvels, Stephane Donnay, Haris Osman, Ingrid Dewolf,
Paru Desphande, Peter Peumans,

imec CMORE-Technology and Lifescience Technology teams



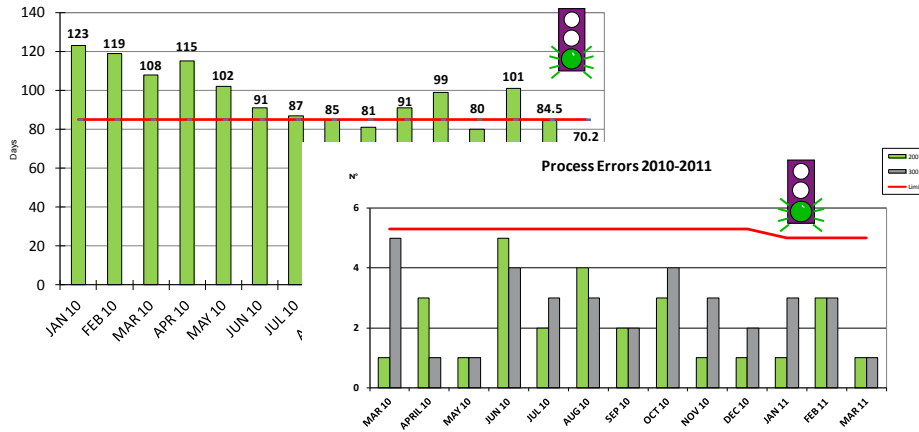
CMORE

THE ROUTE FROM SILICON CONCEPT TO A PRODUCT



CMORE TECHNOLOGY PLATFORMS

Quality and cycle time KPIs

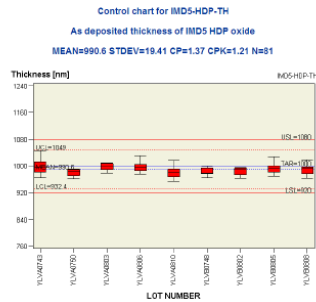


Mature design kits

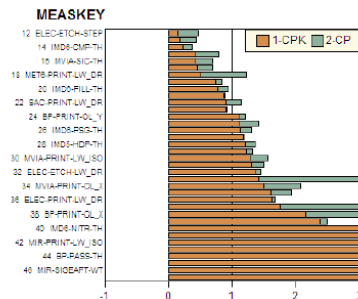
Process description	Layout rules	Material properties	P-cells & Models																																																																																																																																																																																	
<p>Figure 1: The device is coated with photoresist and exposed with the mask (SU-8), after development of the photoresist, the top and bottom layers of photoresist are etched. The top layer is etched with the photoresist mask. The bottom layer is etched with the photoresist mask. The photoresist mask is etched with the photoresist mask.</p>	<p>6.4. Layer 005: ELECTRIC (EL)</p> <table border="1"> <thead> <tr> <th>Layer</th> <th>Material</th> <th>Thickness [nm]</th> <th>Etch selectivity</th> <th>Etch rate [nm/min]</th> </tr> </thead> <tbody> <tr><td>005.1</td><td>EL01</td><td>100</td><td>100</td><td>100</td></tr> <tr><td>005.2</td><td>EL02</td><td>100</td><td>100</td><td>100</td></tr> <tr><td>005.3</td><td>EL03</td><td>100</td><td>100</td><td>100</td></tr> <tr><td>005.4</td><td>EL04</td><td>100</td><td>100</td><td>100</td></tr> <tr><td>005.5</td><td>EL05</td><td>100</td><td>100</td><td>100</td></tr> <tr><td>005.6</td><td>EL06</td><td>100</td><td>100</td><td>100</td></tr> <tr><td>005.7</td><td>EL07</td><td>100</td><td>100</td><td>100</td></tr> <tr><td>005.8</td><td>EL08</td><td>100</td><td>100</td><td>100</td></tr> <tr><td>005.9</td><td>EL09</td><td>100</td><td>100</td><td>100</td></tr> <tr><td>005.10</td><td>EL10</td><td>100</td><td>100</td><td>100</td></tr> <tr><td>005.11</td><td>EL11</td><td>100</td><td>100</td><td>100</td></tr> <tr><td>005.12</td><td>EL12</td><td>100</td><td>100</td><td>100</td></tr> <tr><td>005.13</td><td>EL13</td><td>100</td><td>100</td><td>100</td></tr> <tr><td>005.14</td><td>EL14</td><td>100</td><td>100</td><td>100</td></tr> <tr><td>005.15</td><td>EL15</td><td>100</td><td>100</td><td>100</td></tr> <tr><td>005.16</td><td>EL16</td><td>100</td><td>100</td><td>100</td></tr> <tr><td>005.17</td><td>EL17</td><td>100</td><td>100</td><td>100</td></tr> <tr><td>005.18</td><td>EL18</td><td>100</td><td>100</td><td>100</td></tr> <tr><td>005.19</td><td>EL19</td><td>100</td><td>100</td><td>100</td></tr> <tr><td>005.20</td><td>EL20</td><td>100</td><td>100</td><td>100</td></tr> </tbody> </table>	Layer	Material	Thickness [nm]	Etch selectivity	Etch rate [nm/min]	005.1	EL01	100	100	100	005.2	EL02	100	100	100	005.3	EL03	100	100	100	005.4	EL04	100	100	100	005.5	EL05	100	100	100	005.6	EL06	100	100	100	005.7	EL07	100	100	100	005.8	EL08	100	100	100	005.9	EL09	100	100	100	005.10	EL10	100	100	100	005.11	EL11	100	100	100	005.12	EL12	100	100	100	005.13	EL13	100	100	100	005.14	EL14	100	100	100	005.15	EL15	100	100	100	005.16	EL16	100	100	100	005.17	EL17	100	100	100	005.18	EL18	100	100	100	005.19	EL19	100	100	100	005.20	EL20	100	100	100	<p>8. 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Statistical Process Control

In-line SPC



Monitoring Cp/Cpk

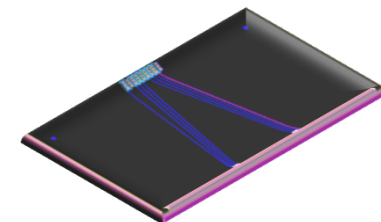
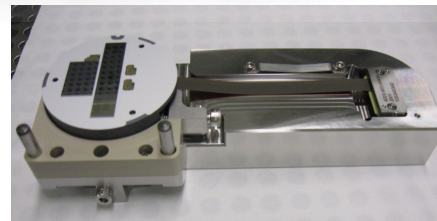
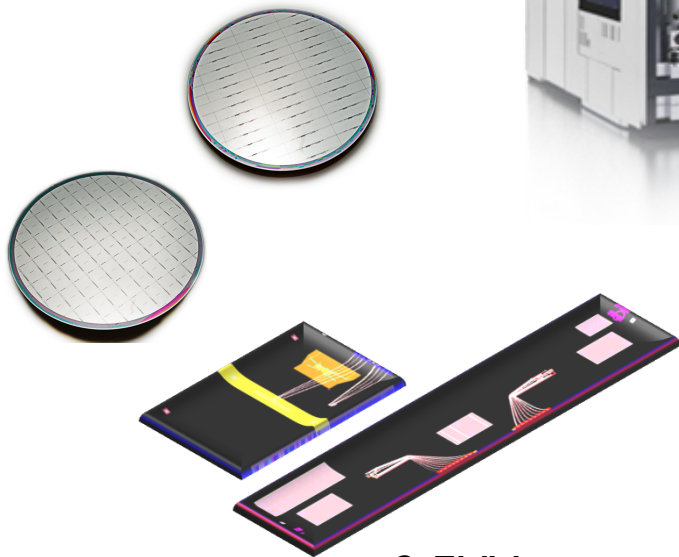


IMEC PRODUCES HIGH-QUALITY EUV SENSORS FOR ASML'S NEXT-GENERATION LITHOGRAPHY TOOLS

3 EUV sensors with superior lifetime and sensitivity

high and direct EUV irradiation doses

CMORE landmark achievement in 2011:
First qualified CMORE chipset installed in customer's product



2 EUV position sensors to calibrate, align and focus lens systems

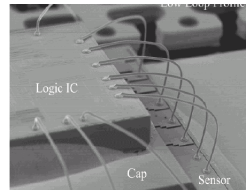
EUV Energy sensor to monitor EUV dose

MEMS TECHNOLOGY VISION

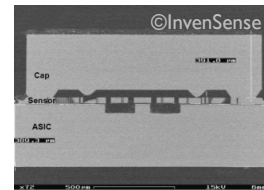
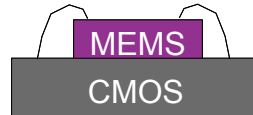
- ▶ Most MEMS devices are single components integrated with separate driver IC chip in multichip package.
- ▶ MEMS technologies are driven towards tighter integration with electronics for better performance, smaller form factors and packaging cost, enabled by:
 - Above IC MEMS
 - 3D Stacking

CMORE SiGeMEMS TECHNOLOGY: I. MONOLITHIC INTEGRATION WITH IC

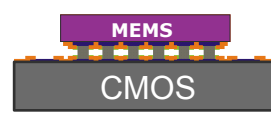
Different MEMS-IC
Integration approaches



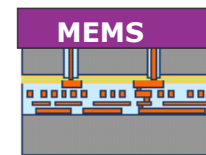
SIP: Stacked die



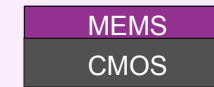
SIP: F2F



SIP: 3D vias



SoC: monolithic



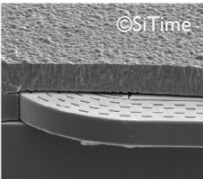
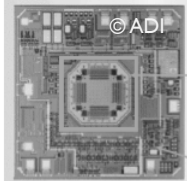
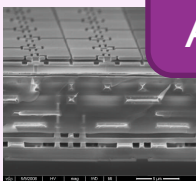

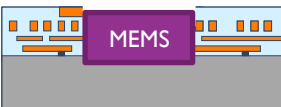

IMEC
Approach

Interconnect pitch	~ 50 um	~10um	~10um	~1um
Interconnect parasitics	few pF	>100fF	<100fF	few fF
yield	KGD	KGD (unless W2W)	KGD (unless W2W)	compound yield

Monolithic approach:

- Most compact solution
- Better intrinsic system reliability: less components, less interconnections
- Best solution for applications that are very sensitive to parasitics
- BUT: MEMS yield is critical

CMORE SiGeMEMS TECHNOLOGY: 2. MEMS LAST (ABOVE CMOS)

Different Monolithic MEMS approaches	 MEMS first	 intraCMOS	 MEMS last
	 MEMS	 MEMS	 MEMS
MEMS processing	No thermal limitations	T-budget 800°C	T-budget 450°C
CMOS	Non-standard	Non-standard	any standard CMOS
Interconnections MEMS-IC	Peripheral around MEMS	Peripheral around MEMS	Distributed & massively parallel

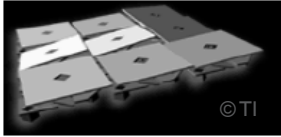
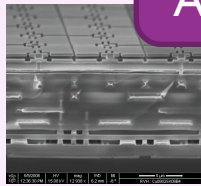
MEMS last:

- most flexible with respect to choice of CMOS technology
- very high-density and massively parallel interconnections possible
→ large arrays of MEMS (e.g. μ mirror arrays)
- BUT: some loss in flexibility (e.g. material choice) due to T-budget

CMORE SiGe MEMS TECHNOLOGY:

3. POLY-SiGe

Different Above CMOS MEMS approaches

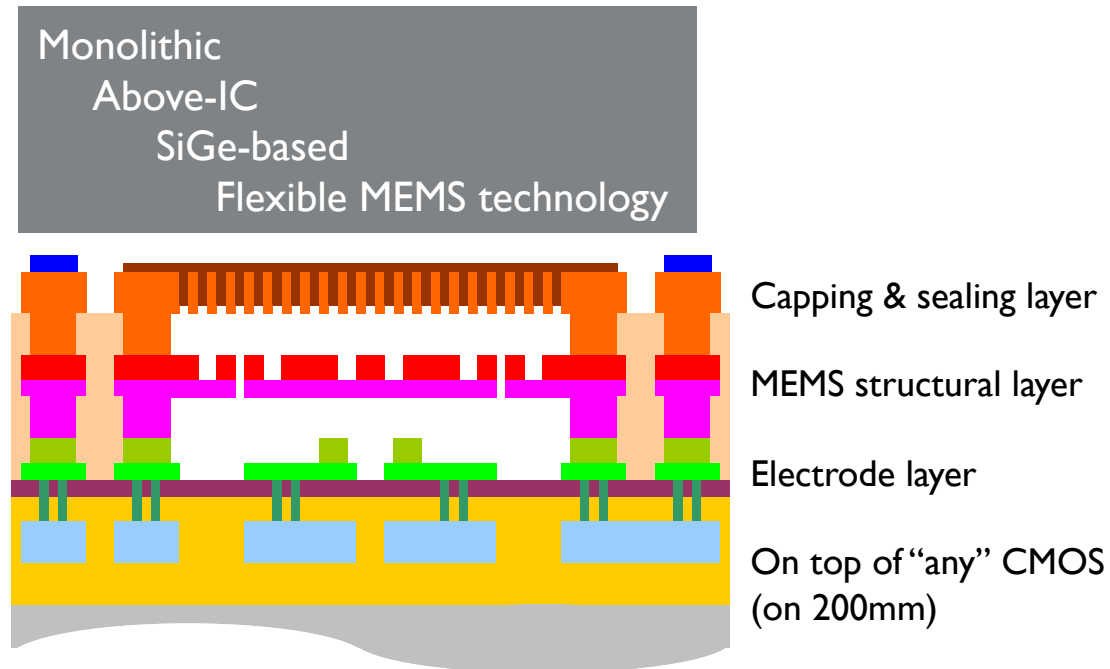
	Al	Poly-SiGe
		 IMEC Approach
Post CMOS integration	yes	yes
Fracture strength [GPa]	0.2	> 2
Mechanical Q	low	> 10.000
Reliability	creep: hinge memory effect	No creep

Poly-SiGe:

- better mechanical properties than Al: higher strength and Q factor
- better reliability properties than Al: less creep and fatigue

CMORE MEMS TECHNOLOGY FOCUS:

4. FLEXIBLE & MODULAR TECHNOLOGY FLOW



Surface micromachining on top of CMOS: temperature limited

450 °C for Al interconnections

Poly-SiGe deposited at 450 °C

$E=140$ GPa (60-70 *at.*% Ge)

Stress = ~0-70 MPa

Strain gradient = $\pm 1 \times 10^{-5}/\mu\text{m}$
(4 μm thick CVD+PECVD SiGe)

Poly-Si: 620 °C deposition, 800 °C needed for desired stress

Flexible and modular technology:

- Variable layer thicknesses
- Application-specific optimization of layer & material properties
- Application-specific functional add-on layers

Imec's SiGe MEMS – PLATFORM

Generic poly-SiGe technology for MEMS:

- “stand-alone” MEMS, or,
- “MEMS above IC” (CMOS-MEMS)

Two structural SiGe layers:

- **MEMS** structural layer (4 μm standard)
- Thin film **capping/packaging** layer (4 μm up to 10 μm thick)

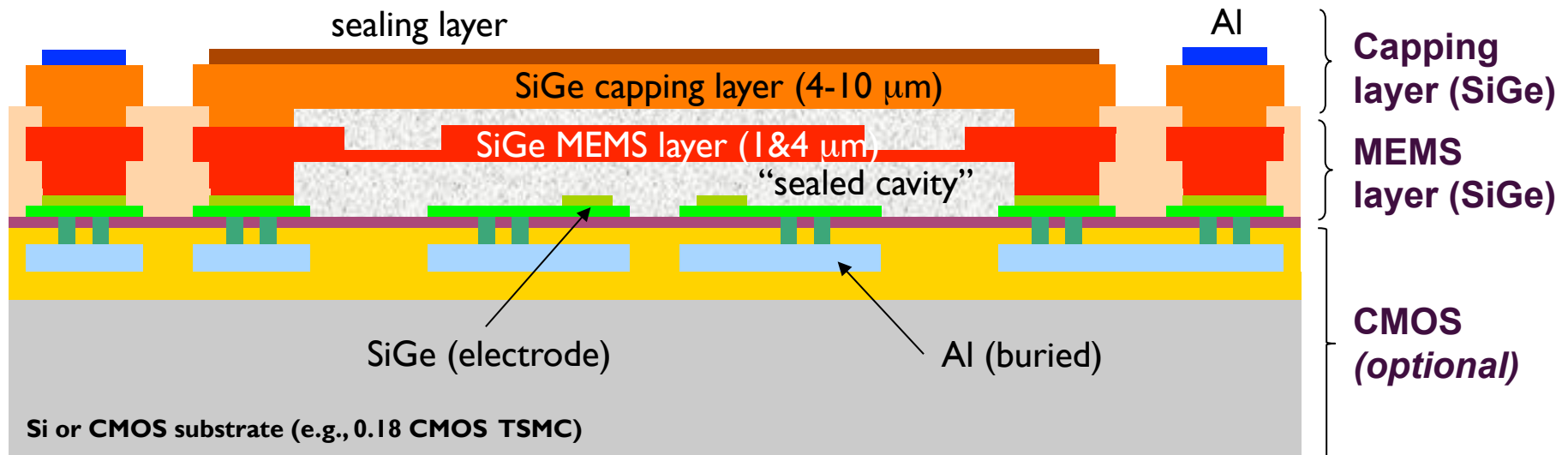
Gap in the SiGe structural layer: 0.5 μm (optional: 0.2 μm)

Low-T processing (< 460°C)

Hermetic package seal (1-100 Pa)

Optional modules:

- Optical (reflective)
- Electrical (metal trace)
- Piezo-resistive layer



FLEXIBILITY WITH LAYER THICKNESSES

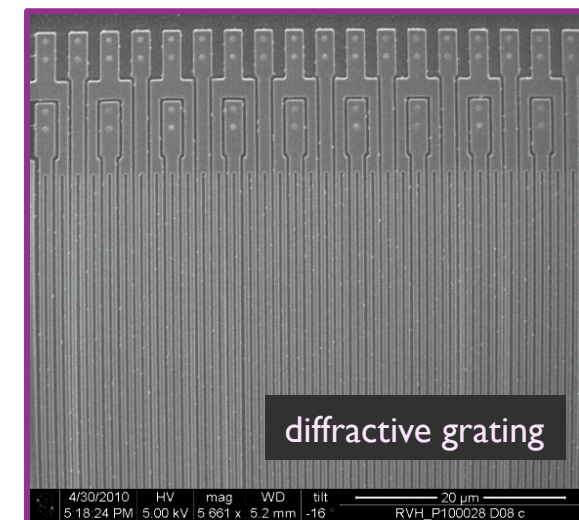
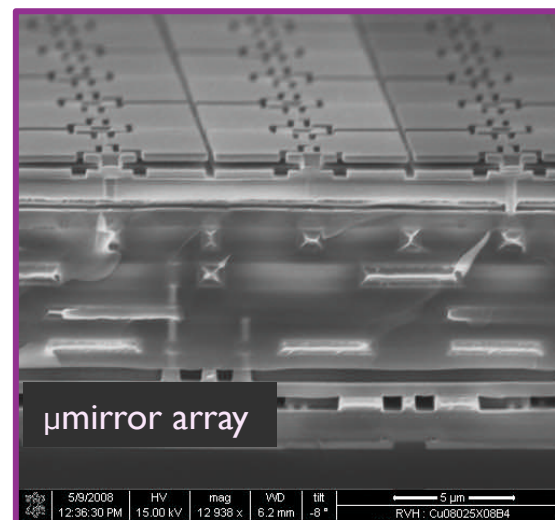
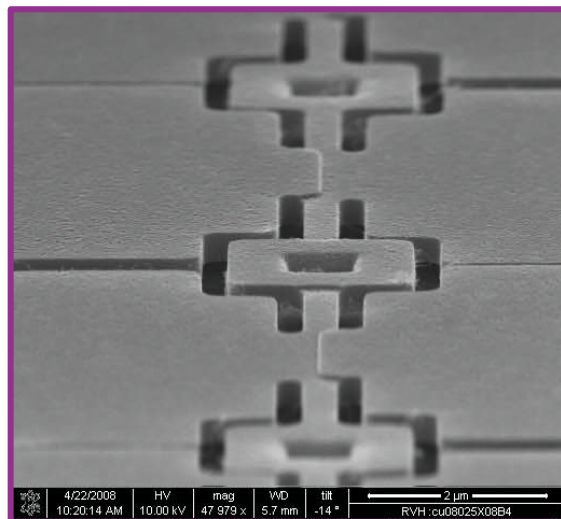
THIN STRUCTURAL LAYER

Thin SiGe platform

- structural layer thickness: **300nm**
- gap: 200→50 nm
- actuation gap: 300 nm
- coating for optical properties

Thin SiGe layers

- stress: 20 MPa tensile
- strain gradient: $1e-4 / \mu\text{m}$
- resistivity: $1\text{m}\Omega\text{cm}$



Typical applications:

- μmirror arrays
- other optical MEMS: e.g. diffractive grating

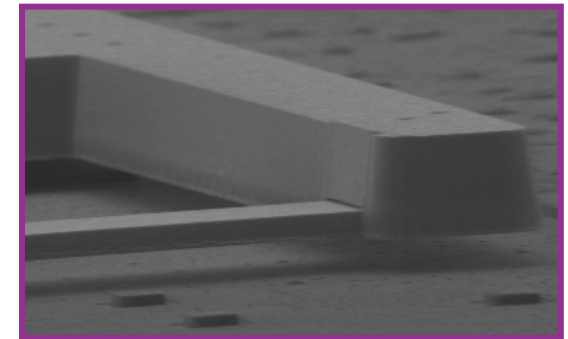
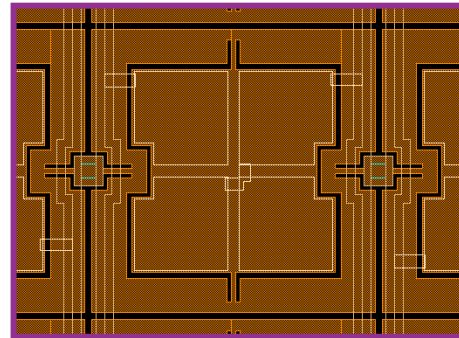
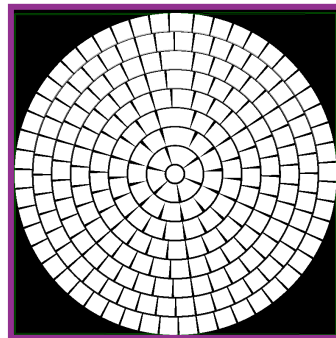
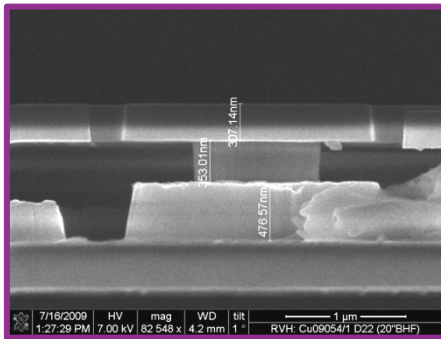
EXPLOITING TECHNOLOGY FLEXIBILITY FOR OPTIMIZED MICROMIRROR DESIGNS

Dual electrode thickness

- mechanical stopper
- reduce actuation voltage

Dual structural layer thickness

- decoupling spring constant and stiffness



Different μ mirror design variants

- Analog vs digital tilt angles
- Circular vs rectangular arrays
- Single-axis vs two-axes mirrors

MODULARITY VIA FUNCTIONAL LAYERS

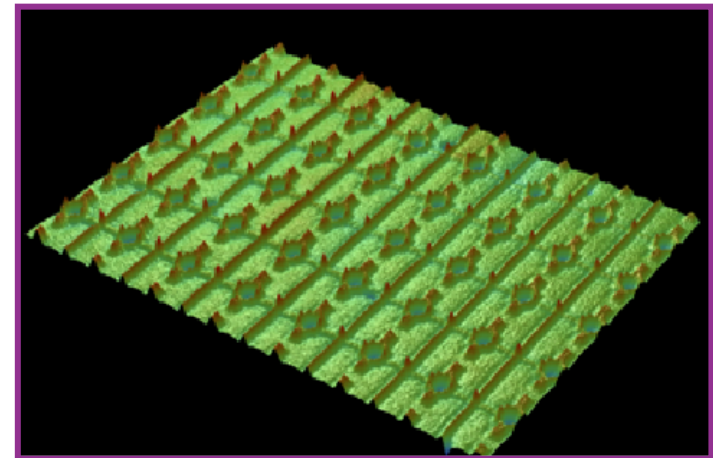
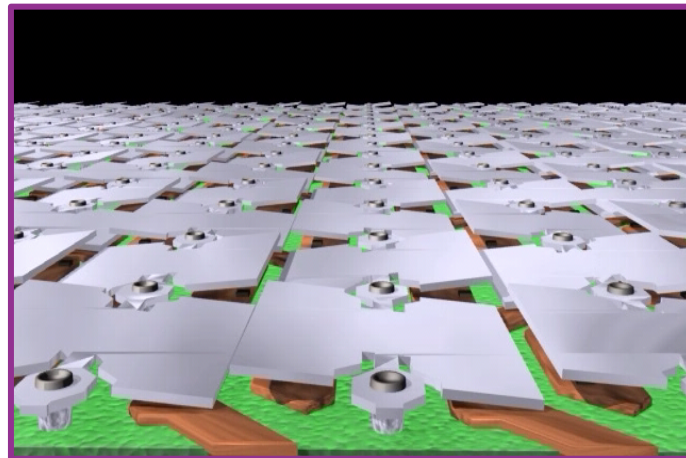
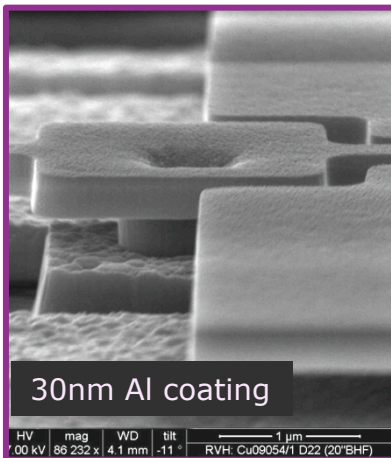
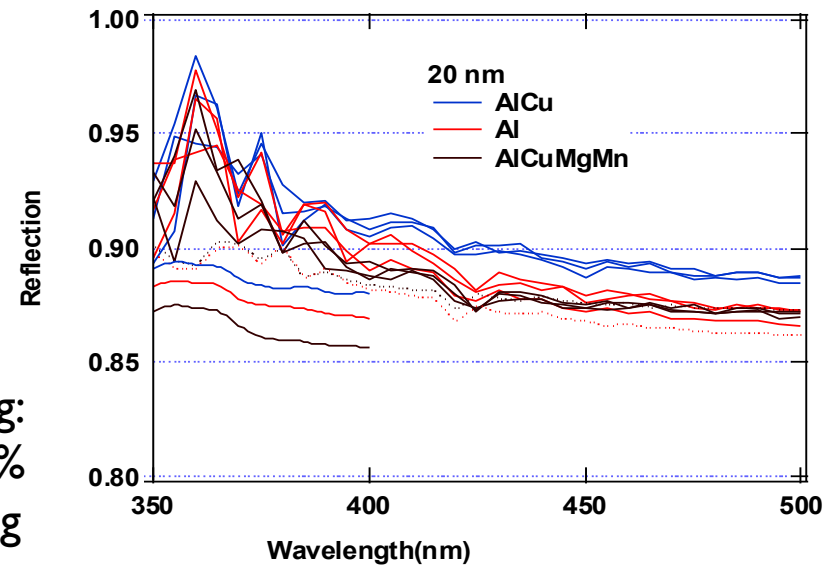
OPTICAL REFLECTIVITY

Different coatings for optical MEMS:

- visual spectrum: 30nm Al coating
- IR applications: Ag coating
- (E)UV applications: Bragg stack

Al coating:

- reflectivity > 85%
- <5nm cupping



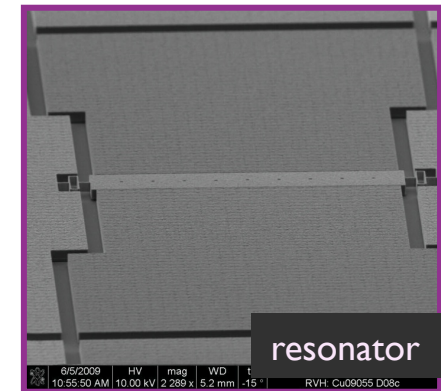
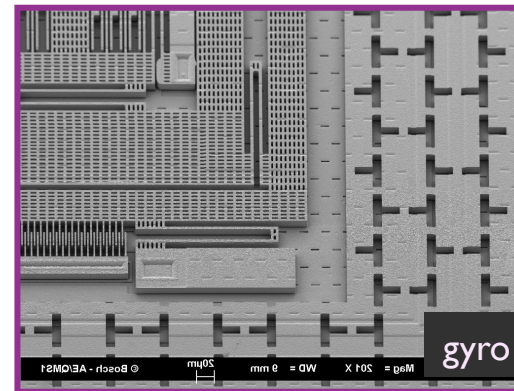
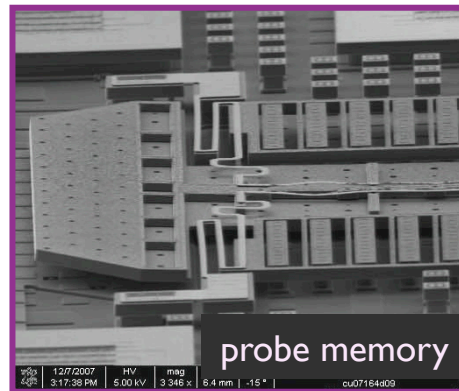
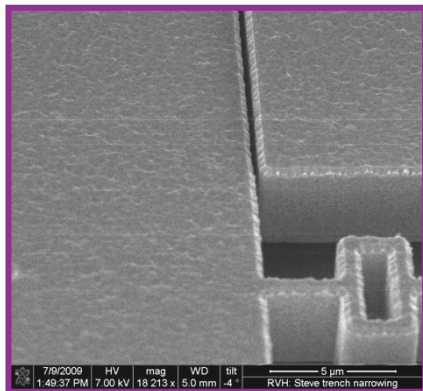
FLEXIBILITY WITH LAYER THICKNESSES

THICK STRUCTURAL LAYER

- “Plain-vanilla” thick SiGe platform
- structural layer thickness: **4 μ m**
 - nanogaps: 500 \rightarrow 200 nm

Thick SiGe layers

- stress: 70 MPa tensile
- strain gradient: $1e-5 / \mu\text{m}$
- resistivity: $1\text{m}\Omega\text{cm}$



Typical applications:

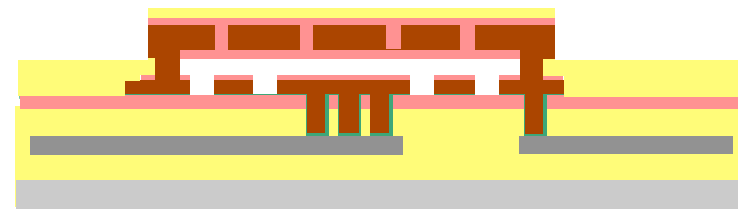
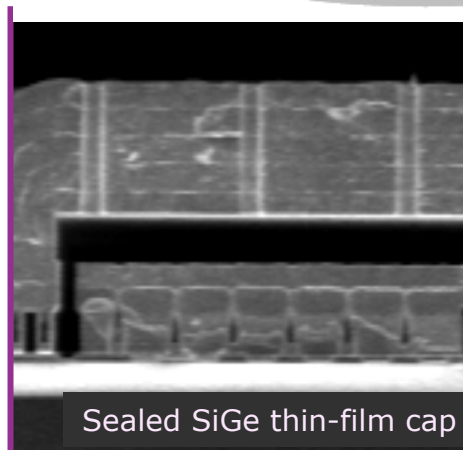
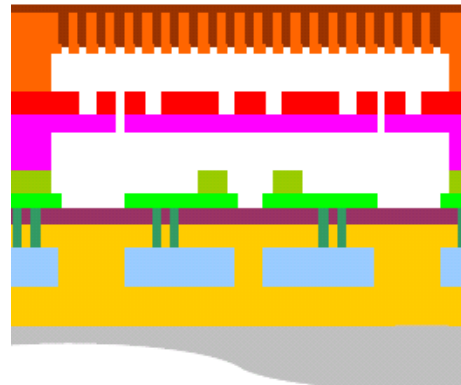
- resonators, **inertial sensors**, actuators, ...
- probe-based memories

MODULARITY VIA FUNCTIONAL LAYERS

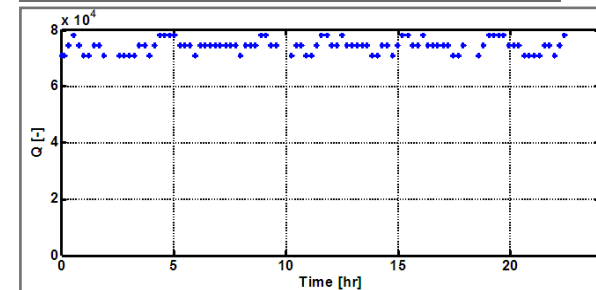
SEALING LAYER

SiGe membranes can be sealed:

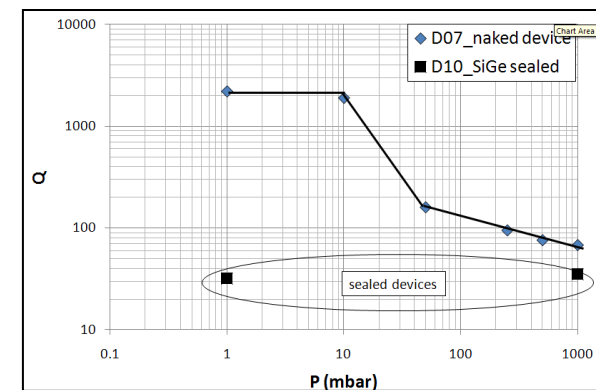
- structural layer
- thin-film capping layer



low pressure sealing of high-Q devices



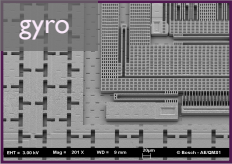
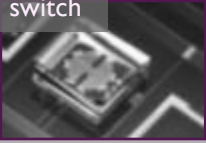




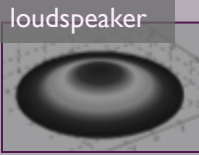
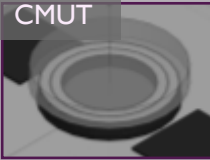
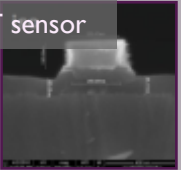

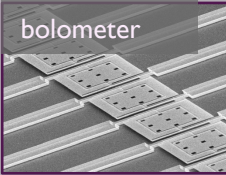
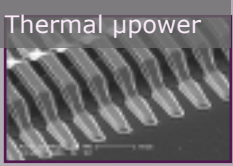
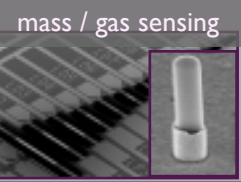

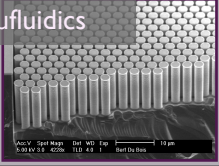
high pressure sealing for low-Q devices



Component applications:

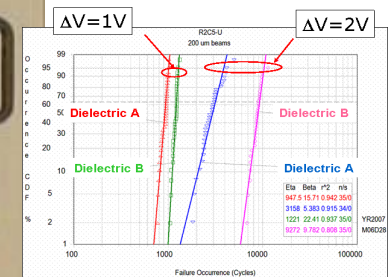
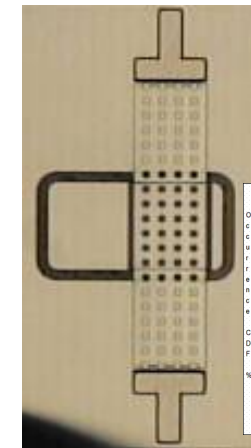
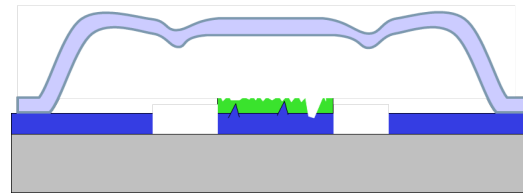
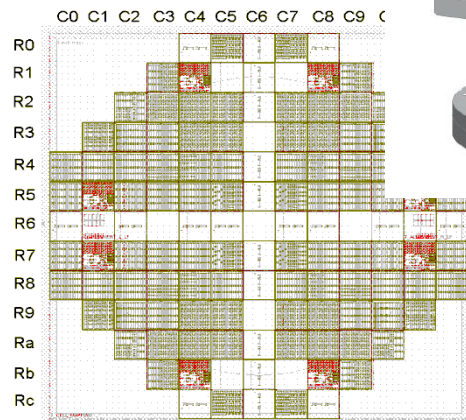
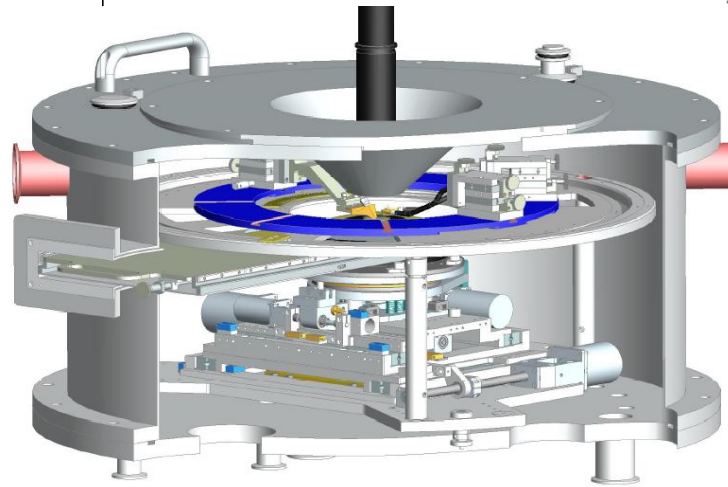
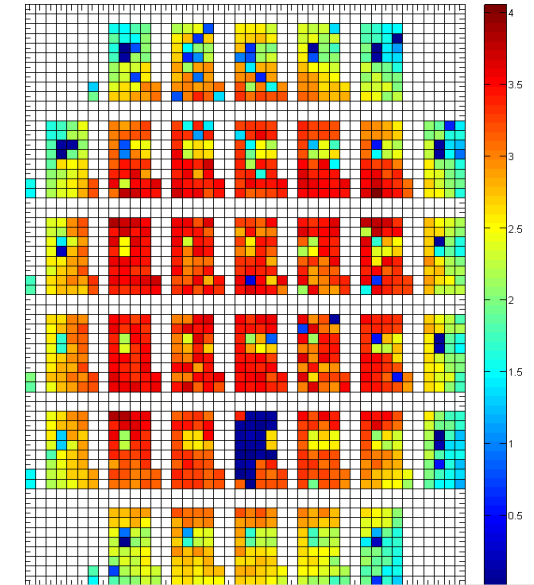
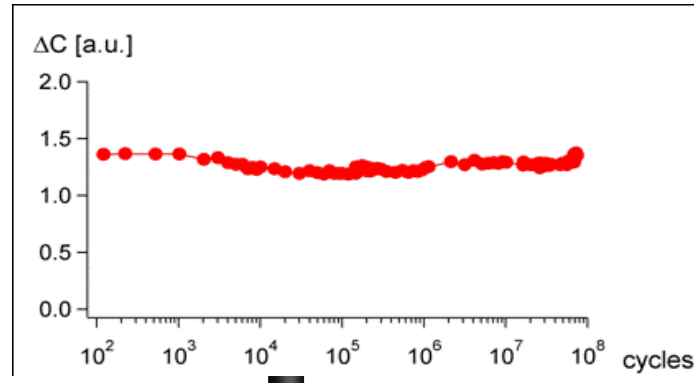
- Capacitive Micromachined Ultrasound Transducers (CMUT)
- Pressure sensors

MEMS APPLICATIONS BUILD ON PLATFORM

	Sensors	Actuators	Imaging & Display	And many other applications ...
Mechanical functionality	gyro 	switch 	μmirror array 	resonator  probe memory 
Acoustic functionality	microphone 	loudspeaker 	CMUT 	
Thermal functionality	T sensor 	micro heater 	bolometer 	Thermal μpower 
Bio / chemical functionality	mass / gas sensing 	μactuator 		μfluidics 

...

STRONG BACKGROUND IN MEMS CHARACTERIZATION AND RELIABILITY



FMEA

CONCLUSIONS

IMEC SIGE MEMSTECHNOLOGY

Monolithic integration with IC

- ▶ Very compact & low cost
- ▶ Allows for higher performance
- ▶ Smaller footprint

SiGe-based above CMOS processing

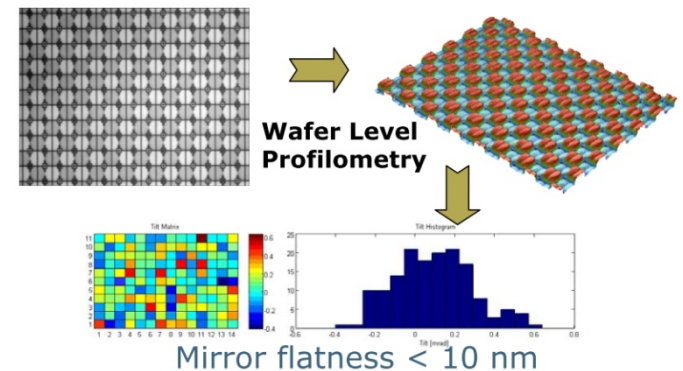
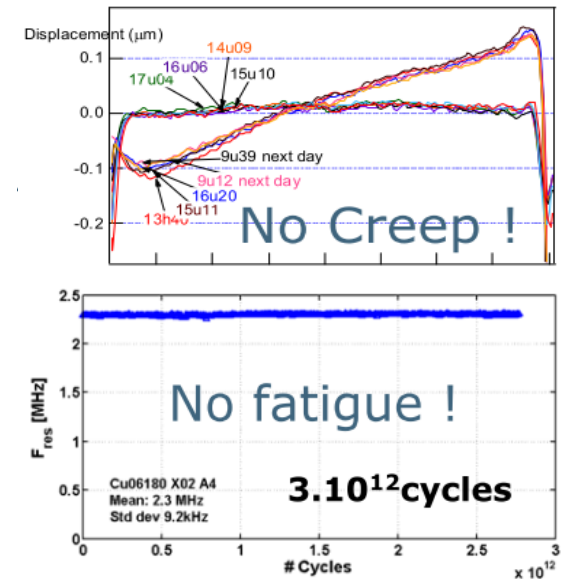
- ▶ High performance: low parasitics
- ▶ Good mechanical properties & reliability
- ▶ Extremely well suited for MEMS array applications

Flexible and Modular

- ▶ Application-specific tuning and optimization
- ▶ Very versatile

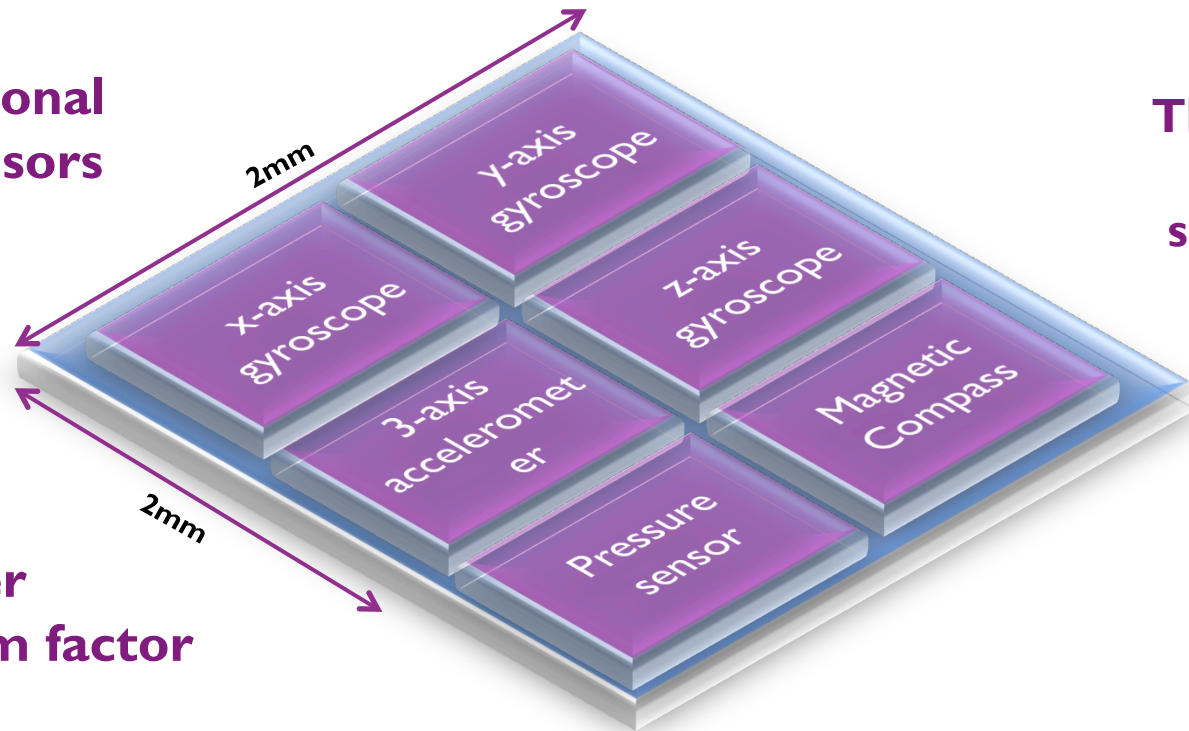
IMEC (TECHNOLOGY) DIFFERENTIATORS

- ▶ Support analog tilting of mirrors
- ▶ Produce micromirrors with reliable performance
 - SiGe mirrors are better material in terms of flexibility than Al (TI umirrors) →
 - No creep
 - No fatigue
 - Flat mirror profiles
- ▶ Produce umirrors with higher performance
 - Smaller mirrors (8umx8um demonstrated)
 - large array sizes (> 10cm²)
 - Large number of mirrors ~ 11M
- ▶ Produce CMOS integrated umirror array
 - Efficient integration of electronic control
 - Efficient control of mirrors



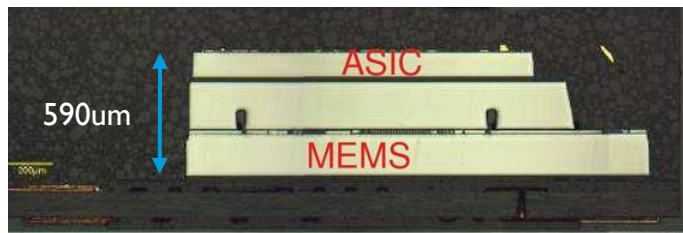
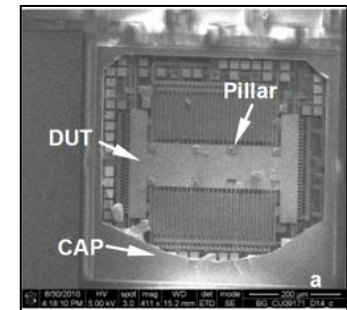
SiGeMEMS ALLOWS FOR MONOLITHIC INTEGRATION OF 10+ DEGREES-OF-FREEDOM INERTIAL MEASUREMENT UNIT

Multi-functional array of sensors

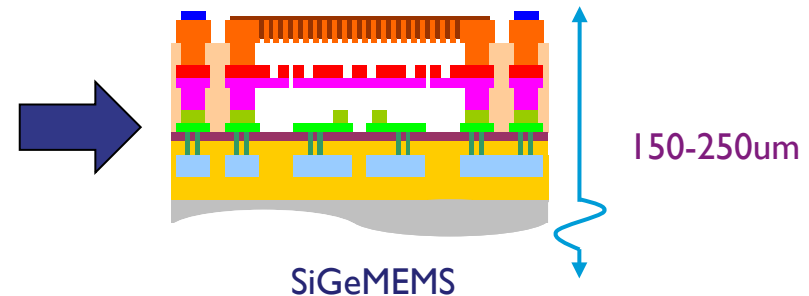


Thin-film capping with different sealing pressures

Low noise
Low power
Small form factor



Traditional Package (©Chipworks)



SiGeMEMS

FROM CMOS TO LIFE SCIENCES TECHNOLOGY



Multidisciplinary teams

Concept development

Process integration
Process technology
Fab operations



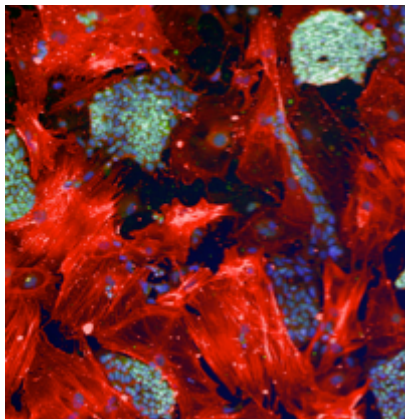
Cell biology
Molecular biology
Surface chemistry
Assay development

From CMOS to life sciences technologies

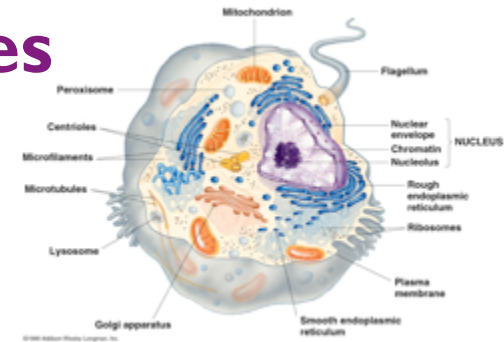


Molecules

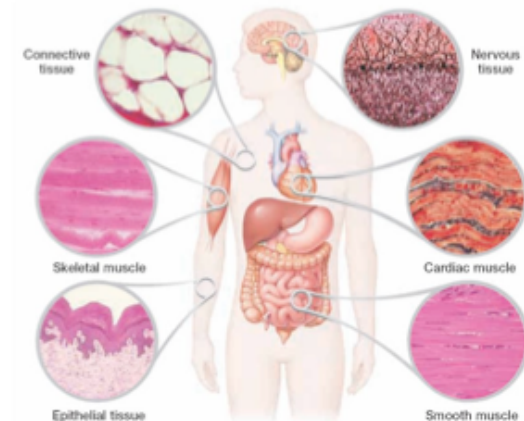
DNA, RNA, proteins, metabolites



Cell cultures



Cells



Tissue

Molecular diagnostics

Cell-based analysis

In vitro systems

In vivo probes

NEXT GENERATION SEQUENCING CHIPS

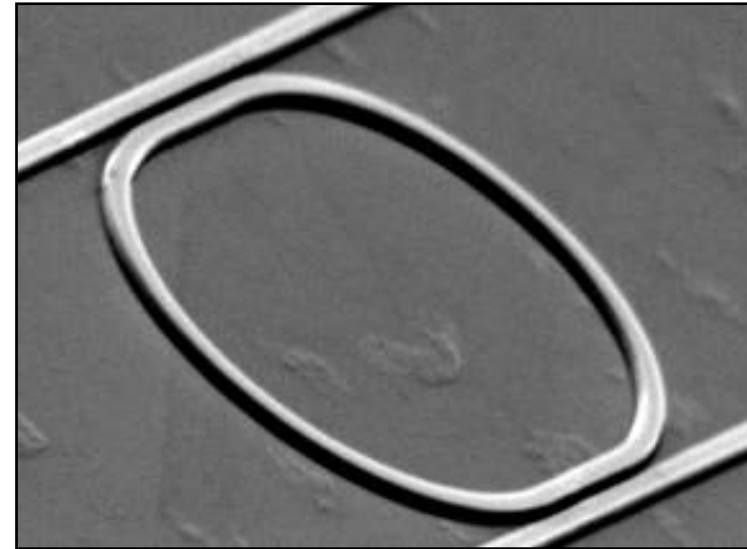
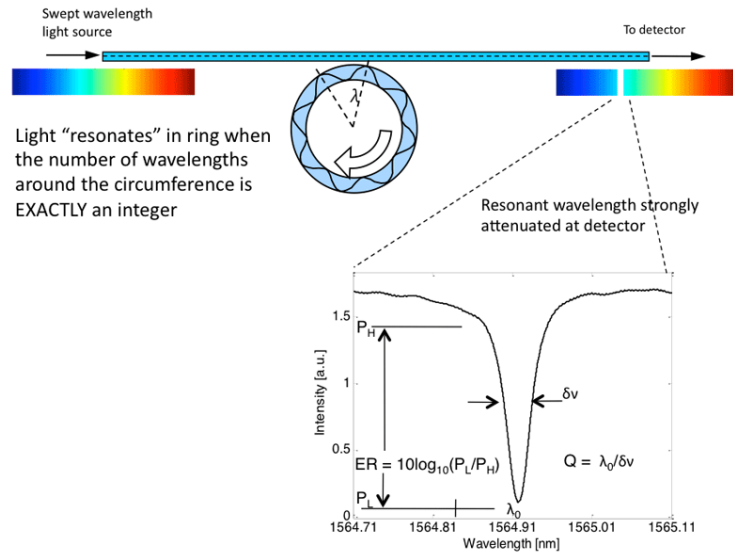
July 23, 2012

Pacific Biosciences and Imec Announce Collaboration to Develop Advanced Microchips for Single Molecule Sequencing Applications

MENLO PARK, Calif., and LEUVEN, Belgium—(BUSINESS WIRE)— Pacific Biosciences of California, Inc. (NASDAQ:PACB) provider of the PacBio® RS High Resolution Genetic Analyzer and Belgium-based nanoelectronics research center imec today announced a multi-year research collaboration focused on the development of advanced microchips for highly multiplexed single molecule genetic analysis. This research and development project will build on Pacific Biosciences' proprietary zero-mode waveguide (ZMW) technology and imec's world-leading expertise in nanophotonics, CMOS sensors, technology integration and fabrication.



GENALYTE BIOSENSOR SILICON PHOTONICS



source www.genalyte.com

Genalyte leverages imec silicon photonics platform to develop and manufacture (low-volume production) its disposable bio-sensor chips.

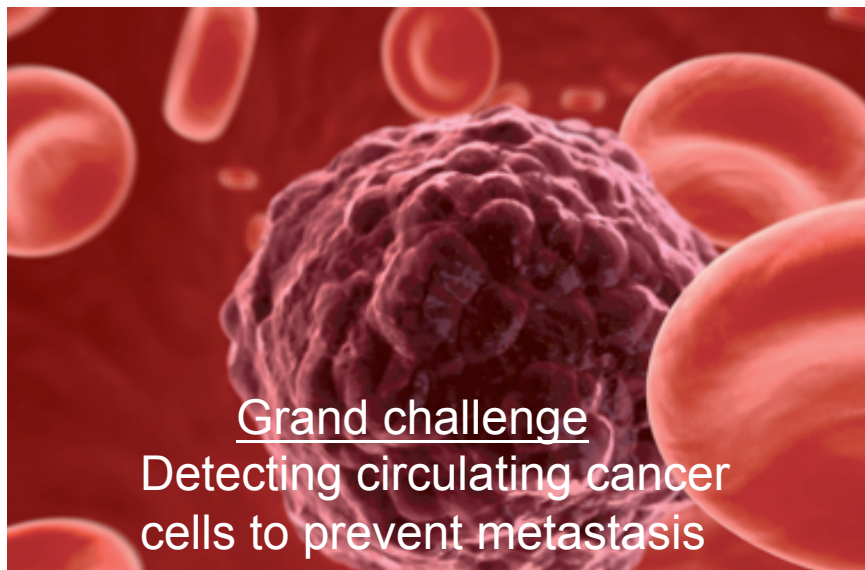


CELL BASED ANALYSIS

Finding individual cells is critical for cancer detection.

- 90% of cancer patients die from metastasis -- the cancer spreads via our circulation system

1 mL of blood contains:
 10^9 blood cells
1 Circulating Tumor Cell

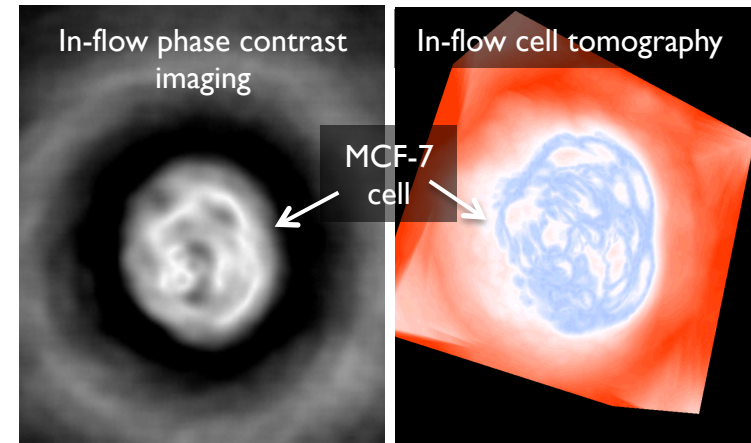


#1 predictor of cancer survival is how early it's detected

HIGH-THROUGHPUT IMAGING FLOW CYTOMETER

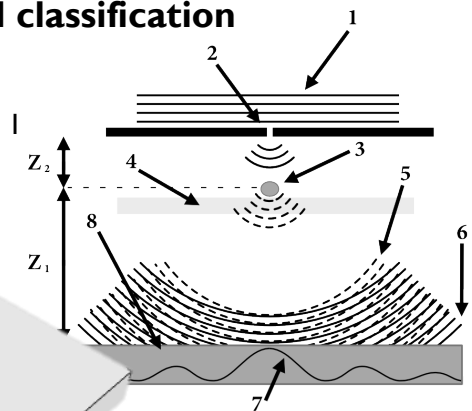
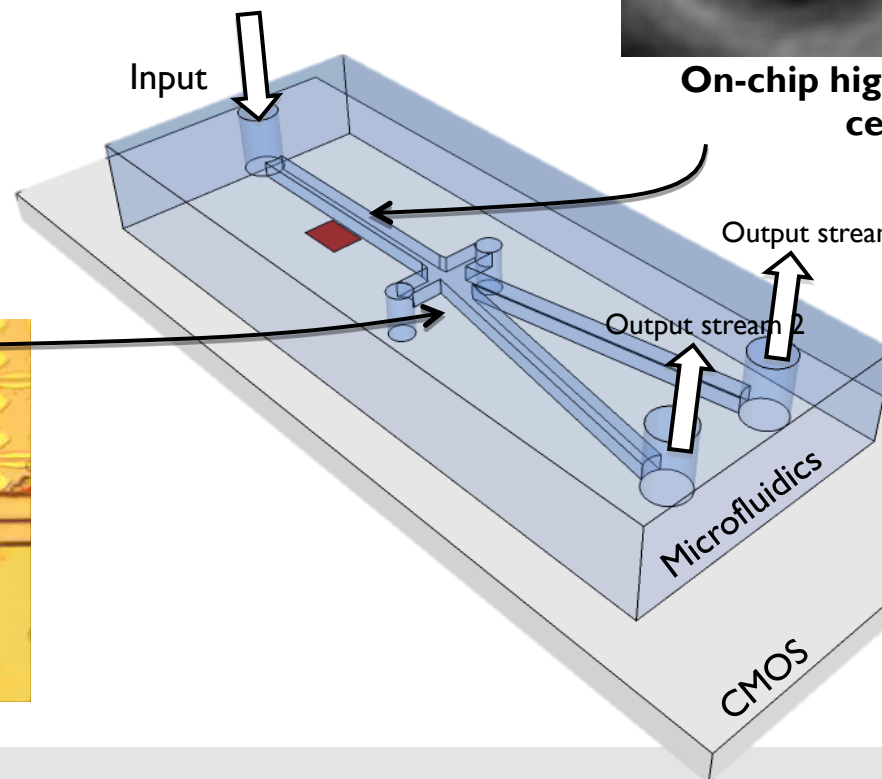
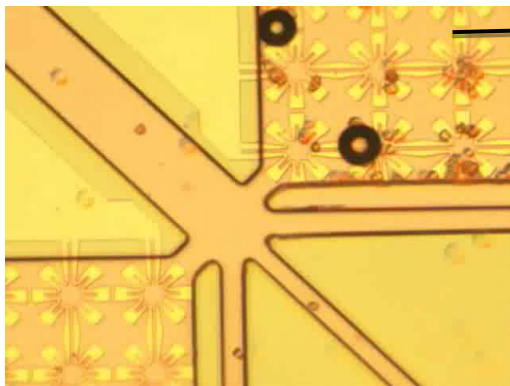
Scalable to 20,000,000 cells/s

>1000-fold improvement over current systems



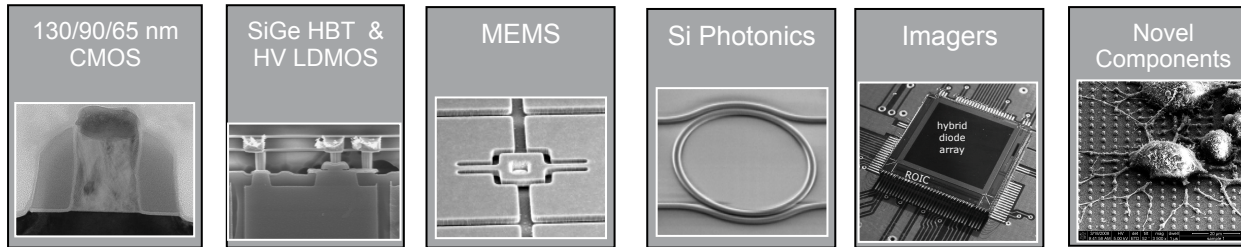
On-chip high-resolution imaging for cell classification

Fast microfluidic bubble-jet cell routing

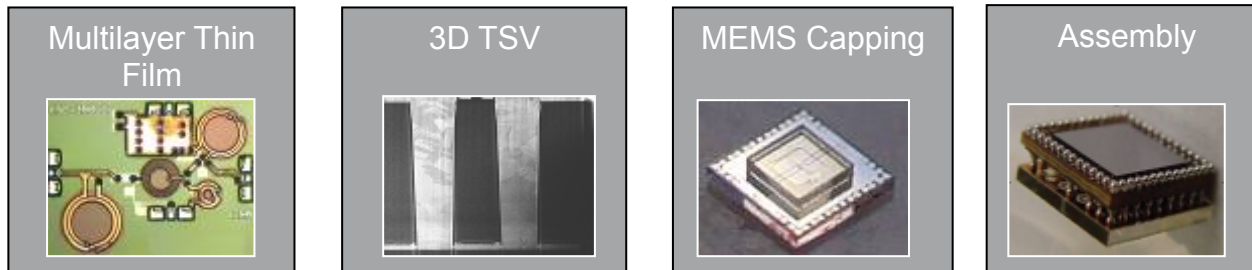


FROM CMOS TO CMORE PLATFORM

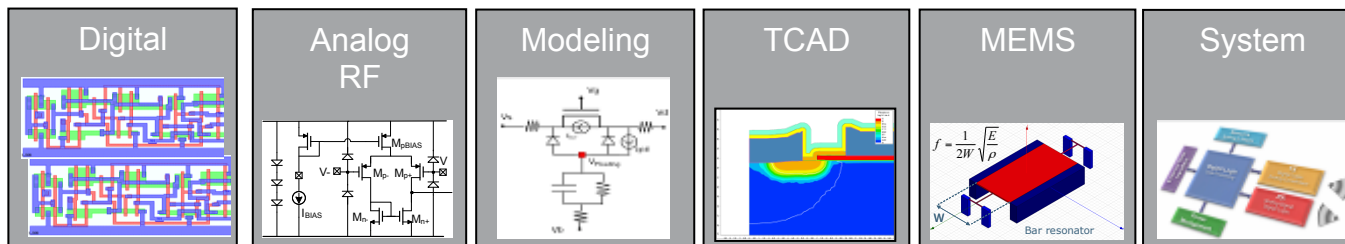
Device Technologies



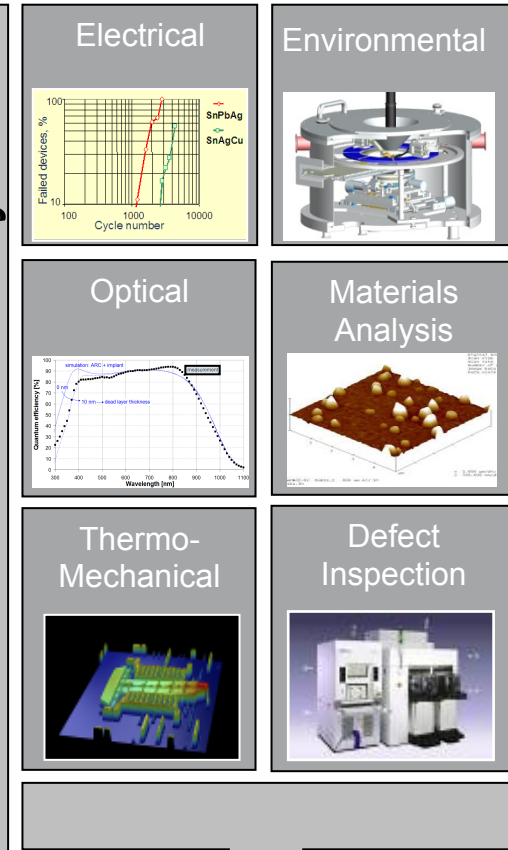
Packaging



Embedded Systems, Design & Software



Test & Reliability



Custom System Solutions



THANK YOU

